Remarks

The Official Action mailed February 21, 2006 rejected claims 1-20. Applicants have amended claim 1 to correct a typo. Claims 1-20 remain pending. Applicants respectfully request allowance of claims 1-20.

Claim Rejections - 35 USC § 102

The Official Action rejected claims 1-3, 5-8 and 12, as being anticipated by Jung-bae Lee et al. (U.S. Patent No. 6,151,271). Applicants respectfully request allowance of claims 1-3, 5-8 and 12.

As is well-established, in order to successfully assert a *prima facie* case of anticipation, the Official Action must provide a single prior art document that includes every element and limitation of the claim or claims being rejected. Therefore, if even one element or limitation is missing from the cited document, the Official Action has not succeeded in making a prima facie case.

Claim 1

Claim 1 requires control logic shared by both the first and second groups of banks of memory, coupled to both the first and second row address decoders, coupled to both the first and second bank selection logics, storing information concerning the state of all banks in the first and second group separately. As discussed in the office action, Jung-bae in his document discloses integrated circuit memory devices which include first and second memory banks, first and second local data lines, a multiplexer, a data selection circuit and a control signal generator. The data selection circuit is provided to route data from the first and second local data lines to the first and second data bus lines, respectively, when a selection

control signal is in a first logic state and routes data from the second and first local data lines to the first and second data bus lines, respectively, when a selection control signal is in a second logic state opposite the first logic state. The control signal generator generates the selection control signal in the first and second logic states when a first address in a string of burst addresses is even and odd. Jung-bae also teaches construction of DRAM which includes a plurality of memory cell arrays and each memory cell arrays include a plurality of memory cell sub- arrays. However, Applicants have been unable to locate where Jung-bae teaches control logic shared by both the first and second groups of banks of memory, coupled to both the first and second row address decoders, coupled to both the first and second bank selection logics, storing information concerning the state of all banks in the first group, including the first bank, and separately storing information concerning the state of all banks in the second group, including the second bank.

The Office Action appears to rely upon the data selection circuit and/or the control signal generator for a teaching of control logic shared by both the first and second groups of memory banks as required by the Applicants' invention of claim 1. Jung-bae discloses the data selection circuit provided to route data from the local data lines to the data bus lines and the control generator provided to generate the selection control signals in the first and second logic states. Whereas according to the applicants' invention, the control logic may be shared by both the groups of banks of memory and may store information concerning the state of all banks in the first group and second group separately. Applicants submit that a person skilled in the art shall not consider the data selection circuit and/or the control signal generator similar to the control logic shared by both the first and second groups of memory banks.

Since, Jung-bae does not teach each and every element of Applicants' claim 1, Jung-bae does not anticipate Applicants' claim 1. Applicants respectfully request that the rejection of claim 1 be withdrawn.

If the Examiner elects to maintain the present rejection, Applicants respectfully request that the Examiner indicate with specificity (e.g. column and line) what in the teachings of Jung-bae is being equated with control logic shared by both the first and second groups of banks of memory, coupled to both the first and second row address decoders, coupled to both the first and second bank selection logics.

Claims 2, 3 and 5

Claims 2, 3 and 5 include claim 1 as a base claim. Accordingly, claims 2, 3 and 5 are allowable for at least the reasons stated above in regard to claim 1. Additional points could be made in support of the allowance of claims 2, 3 and 5. However, Applicants believe the above is sufficient to overcome the present rejection of claims 2, 4 and 5 under Jung-bae. Accordingly, such arguments will not be presented at this time so as to not burden the Examiner with the review of superfluous points. Applicants respectfully request that the rejection of claims 2, 4 and 5 be withdrawn.

Claim 6

Claim 6 requires control logic shared by both the first and second groups and having both a first state logic storing information concerning the state of all banks in the first group and a second state logic storing information concerning the state of all banks in the second group. Jung-bae in his document discloses integrated circuit memory devices which include first and second memory banks, first and second local data lines, a multiplexer, a data selection circuit and a control signal generator.

Jung-bae also teaches construction of DRAM which includes a plurality of memory cell arrays and each memory cell arrays include a plurality of memory cell sub-arrays. However, Applicants have been unable to locate where Jung-bae teaches control logic shared by both the first and second groups and having both a first state logic storing information concerning the state of all banks in the first group and a second state logic storing information concerning the state of all banks in the second group. Applicants submit that Jung-bae does not discloses control logic shared by both the first and second groups and having both a first state logic storing information concerning the state of all banks in the first group and a second state logic storing information concerning the state of all banks in the second group.

Since, Jung-bae does not teach each and every element of Applicants' claim 1, Jung-bae does not anticipate Applicants' claim 1. Applicants respectfully request that the rejection of claim 1 be withdrawn.

If the Examiner elects to maintain the present rejection, Applicants respectfully request that the Examiner indicate with specificity (e.g. column and line) what in the teachings of Jung-bae is being equated with control logic shared by both the first and second groups of banks of memory, coupled to both the first and second row address decoders, coupled to both the first and second bank selection logics.

Claims 7, 8 and 12

Claims 7, 8 and 12 include claim 6 as a base claim. Accordingly, claims 7, 8 and 12 are allowable for at least the reasons stated above in regard to claim 6. Additional points could be made in support of the allowance of claims 7, 8 and 12. However, Applicants believe the above is sufficient to overcome the present rejection of claims 7, 8 and 12 under Jung-bae. Accordingly, such arguments will not be

presented at this time so as to not burden the Examiner with the review of superfluous points. Applicants respectfully request that the rejection of claims 7, 8 and 12 be withdrawn.

Claim Rejections - 35 USC § 103 (Jung-bae Lee/Ho-Cheol Lee)

The Official Action rejected claims 4, 9 and 11 under 35 U. S. C. 103(a) as being unpatentable over Jung-bae Lee as applied to claim 1 and 6 above, further in view of Ho-Cheol Lee (US Patent 6,279,116B1). Applicants respectfully request the rejection of claims 4, 9 and 11 be withdrawn.

Claims 4 and 11

Claims 4 and 11 include claim 1 and claim 6 as a base claim, respectively. Accordingly, claims 4 and 11 are allowable for at least the reasons stated above in regard to claims 1 and 6. Furthermore, claims 4 and 11 require control logic to store information concerning which rows are open in all banks in the first group separately from information concerning which rows are open in all banks in the second group. As discussed in the office action, Application submit that Ho-Cheol discloses row control circuit meant for generating signals or clocks for selecting word line during time period of t.sub.RCD, developing to bit lines information data. However, Ho-Cheol does not teach storing the signals or clocks generated by the row control circuit regarding row opening to let the system know that particular row is open and thus it can not guide the operation of the control circuit during next cycle of the operation. Whereas, according to the Applicants' invention, the information regarding the row is stored and the read/write operation is directed to the intended row by the control logic as required by Applicants' invention of claims 4 and 11.

Since, the proposed combination does not teach each and every element of Applicants' claims 4 and 11, the proposed combination does not arrive at the invention of the Applicants' claims 4 and 11. Applicants respectfully request that the rejection of claims 4 and 11 be withdrawn.

Claim 9

Claim 9 include claim 6 as a base claim. Accordingly, claim 9 is allowable for at least the reasons stated above in regard to claim 6.

Claim Rejections - 35 USC § 103 (Jung-bae Lee/Carnevale)

The Official Action rejected claim 10 under 35 U. S. C. 103 (a) as being unpatentable over Jung-bae Lee as applied to claim 6 and 9 above, further in view of Carnevale et al. (US Patent 5,721,874). Applicants respectfully request the rejection of claim 10 be withdrawn.

Claim 10

Claim 10 includes claim 6 as a base claim. Accordingly, claim 10 is allowable for at least the reasons stated above in regard to claim 6. Furthermore, claim 10 requires memory controller incorporates a control storage to maintain information concerning the size of a cache line within the cache. Application submit that Carnevale teaches a page table arrangement for storing cache characteristic information and a cache line characteristic data, but Carnevale does not appear to teach a memory controller incorporating a control storage to maintain information concerning the size of cache line within the cache. Further, Jung-bae also does not appear to teach that memory controller incorporates a control storage to maintain information concerning the size of a cache line within the cache.

Since, the proposed combination does not teach memory controller incorporates a control storage to maintain information concerning the size of a cache line within the cache as required by the Applicants' claim 10, the proposed combination does not arrive at the invention of the Applicants' claim 10. Applicants respectfully request that the rejection of claim 10 be withdrawn.

Claim Rejections - 35 USC § 103 (Jung-bae Lee/Kopet)

The Official Action rejected claim 13-15 under 35 U. S. C. 103 (a) as being unpatentable over Jung-bae Lee as applied to claim 6 and 12 above, further in view of Kopet et al. (US Patent 5,448,310). Applicants respectfully request the rejection of claim 13 be withdrawn.

Claim 13

Claim 13 includes claim 6 as a base claim. Accordingly, claim 13 is allowable for at least the reasons stated above in regard to claim 6. Furthermore, claim 13 requires the memory controller signals the memory IC that both the first and second read transactions are to be terminated early at a quantity of bytes less than the quantity of bytes that the memory IC normally fetches internally for a read transaction. As discussed in the office action, Kopet teaches the difference between mode 1 and mode 0 burst read cycles and assertion and deassertion of different modes so as to terminate the cycle. However, Applicants have been unable to locate where Kopet teaches the memory controller signals the memory IC that both the first and second read transactions are to be terminated early at a quantity of bytes less than the quantity of bytes that the memory IC normally fetches internally for a read transaction, wherein the memory controller times the first and second read transactions to minimize the time that elapses between the end of the actual transfer

of bytes across the memory bus for the first read transaction and the beginning of the actual transfer of bytes across the memory bus for the second read transaction.

Further, as admitted in the office action Jung-bae also does not appear to teach the memory controller signals the memory IC that both the first and second read transactions are to be terminated early at a quantity of bytes less than the quantity of bytes that the memory IC normally fetches internally for a read transaction.

Since, the proposed combination does not teach the memory controller signals the memory IC that both the first and second read transactions are to be terminated early at a quantity of bytes less than the quantity of bytes that the memory IC normally fetches internally for a read transaction as required by the Applicants' claim 13, the proposed combination does not arrive at the invention of the Applicants' claim 13. Applicants respectfully request that the rejection of claim 13 be withdrawn.

Claims 14-15

Claims 14-15 include claim 13 as a base claim. Accordingly, claims 14-15 are allowable for at least the reasons stated above in regard to claim 13. Additional points could be made in support of the allowance of claims 14-15. However, Applicants believe the above is sufficient to overcome the present rejection of claims 14-15 under Jung-bae and Kopet. Accordingly, such arguments will not be presented at this time so as to not burden the Examiner with the review of superfluous points. Applicants respectfully request that the rejection of claims 14-15 be withdrawn.

Claim Rejections - 35 USC § 103 (Jung-bae Lee/IBM)

The Official Action rejected claim 16 under 35 U. S. C. 103 (a) as being unpatentable over Jung-bae Lee, further in view of non-patent literature "Bit Vector Algorithm for detecting Self-Data Chains" (hereafter referred as "IBM"). Applicants respectfully request the rejection of claim 13 be withdrawn.

Claim 16

Claim 16 requires waiting a period of time appropriate to prevent conflicts between transfers of bytes for the first and second read operations and to minimize the amount of time between the ends of the burst transfer of data for the first read operation to the beginning of the burst transfer of data for the second read operation.

It is well established that obviousness requires a teaching or a suggestion by the relied upon prior art of all the elements of a claim (M.P.E.P. §2142). Without conceding the appropriateness of the combination, Applicants respectfully submit that the combination of Jung-bae Lee and IBM does not meet the requirements of an obvious rejection in that neither teaches nor suggests waiting a period of time appropriate to prevent conflicts between transfers of bytes for the first and second read operations and to minimize the amount of time between the ends of the burst transfer of data for the first read operation to the beginning of the burst transfer of data for the second read operation. As admitted in the office action, neither Jung-bae nor IBM teaches the above limitation of the Applicants' claim 16 and thus does not arrive at the claimed invention of claim 16.

However, the Official Action indicates without citing any legal precedent that a sequence in which things must occur does not change the purpose or functionality of the claimed invention. The above statement appears to infer that the above

indicated limitation of claim 16 has no effect on the functionality of the claimed invention. However, the above limitation is more than just changing the order of various steps. The limitation to wait for an appropriate time has been introduced between the steps of transmitting a first read command and second read command so as to prevent the conflict between transfer of bytes for the first and second read operations. Thus, the limitation of claim 16 addresses a conflict not taught or suggested by the cited references.

Therefore, Applicants submit that the proposed combination does not arrive at the claimed invention nor render the claimed invention otherwise obvious. Applicants respectfully request the rejection of claim 16 be withdrawn.

Claim Rejections - 35 USC § 103 (Jung-bae Lee/IBM/Carnevale)

The Official Action rejected claim 17 under 35 U. S. C. 103 (a) as being unpatentable over Jung-bae Lee and IBM as applied to claim 16 above, further in view of Carnevale et al. (US Patent 5,721,874). Applicants respectfully request the rejection of claim 17 be withdrawn.

Claim 17

Claim 17 includes claim 16 as a base claim. Accordingly, claim 17 is allowable for at least the reasons stated above in regard to claim 16. Furthermore, claim 17 requires checking stored information concerning the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in the memory IC in determining the quantity of bytes to which each transfer of data will be limited for both the first and second read operations. Carnevale teaches a page table arrangement for storing cache characteristic information for controlling cache access. However, Carnevale does not teach a process to check stored

information relating to the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in the memory IC in determining the quantity of bytes to which each transfer of data will be limited for both the first and second read operations. Further and as admitted, Jung-bae and IBM fail to teach the limitation of the Applicants' claim 16.

Therefore, the proposed combination does not arrive at the claimed invention since the proposed combination does not teach or suggest each and every limitation of claim 17. Applicants respectfully request the rejection of claim 17 be withdrawn.

Claim Rejections - 35 USC § 103 (Jung-bae Lee/IBM/Kopet)

The Official Action rejected claims 18 and 19 under 35 U. S. C. 103 (a) as being unpatentable over Jung-bae Lee and IBM as applied to claim 16 above, further in view of Kopet et al. (US Patent 5,448,310). Applicants respectfully request the rejection of claims 18 and 19 be withdrawn.

Claim 18 and 19

Claims 18 and 19 includes claim 16 as a base claim. Accordingly, claim 18 and 19 are allowable for at least the reasons stated above in regard to claim 16. Furthermore, the above discussion regarding claim 13 is relevant to the patentability of claim 18 and 19. Withdrawal of the present rejection of claims 18 and 19 is respectfully requested.

Claim Rejections - 35 USC § 103 (Kopet/Ho-Cheol Lee/Keskar/Carnevale/IBM)

The Official Action rejected claim 20 under 35 U. S. C. 103 (a) as being unpatentable over Kopet et al. further in view of Ho-Cheol Lee , Keskar et al., Carnevale and the non-patent literature "Bit Vector Algorithm for detecting Self-Data

Chains" (hereafter referred as "IBM"). Applicants respectfully request the rejection of claim 20 be withdrawn.

Claim 20

Claim 20 requires checking stored information concerning the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in the memory IC in determining the quantity of bytes to which each transfer of data will be limited for both the first and second read operations.

As is well established, a prima facie showing of obviousness may only be established if there is a clear suggestion from or in the prior art to make the modifications proposed by the Examiner. *See Gillette Co. v. S.C. Johnson & Son, Inc.* 919 F. 2d 720 (Fed Cir. 1990). Applicants submit that there is no clear suggestion or motivation, in the light of the cited references, for a person to combine the references. The Official Action appears to combine the "Motion Estimation Coprocessor" of Kopet, the "Synchronous Dynamic Random Access Memory Device" of Ho-Cheol Lee, the "Programmable Memory Controller" of Keskar, the "Configurable Cache" of Carnevale and IBM's "Bit Vector Algorithm" in order to propose a memory IC having control logic shared by both the first and second groups of banks of memory, coupled to both the first and second row address decoders, coupled to both the first and second bank selection logics, storing information concerning the state of all banks in the first and second group separately. Despite the broad statement made by the Examiner, there appears to be no reason why one skilled in the art, in light of these references, would make the proposed combination.

Carnevale teaches a page table arrangement for storing cache characteristic information for controlling cache access. However, Carnevale does not teach a

process to check stored information relating to the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in the memory IC in determining the quantity of bytes to which each transfer of data will be limited for both the first and second read operations.

Applicants submit that there is no suggestion or motivation, in the light of the cited references, for a person skilled in the art to combine the references. Therefore, a prima facie case of obviousness in regard to claim 20 has not been established. Applicants respectfully request the rejection of claim 20 be withdrawn.

Conclusion

The foregoing is submitted as a full and complete response to the Official Action. Applicants submit that all remaining claims are in condition for allowance. Reconsideration is requested, and allowance of all remaining claims is earnestly solicited.

Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666. If the Examiner believes that there are any informalities which can be corrected by an Examiner's amendment, a telephone call to the undersigned at (503) 439-8778 is respectfully solicited.

Respectfully submitted,

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